CLAIMS

1. A semiconductor testing apparatus including a function which applies a predetermined direct current to an IC pin of a device under test (DUT) and measures a current flowing at this moment, comprising:

an applied voltage source which applies a predetermined constant voltage to the DUT;

current/voltage converting means for directly inserting a predetermined resistance between an output end of the applied voltage source and the IC pin of the DUT, and converting a quantity of the current flowing through the DUT into a voltage; and

when a voltage at the output end of the applied voltage source is a common mode voltage, a voltage applied to the DUT through the current/voltage converting means is a detection voltage, and a difference between the both voltages is a potential difference,

current measuring means for switching and receiving the common mode voltage and the detection voltage in time series, shifting each received voltage to a predetermined low voltage, and respectively outputting low-voltage measurement data obtained by receiving each shifted voltage and subjecting the received voltage to quantization conversion.

2. The semiconductor testing apparatus according to claim 1, wherein the applied voltage source comprises a first DA converter and a first operational amplifier,

the first DA converter generates a predetermined

reference voltage based on set data which is set from the outside,

the first operational amplifier is an operational amplifier for a power, receives the reference voltage at a positive input end thereof, receives a test voltage which is supplied to the DUT at a negative input end thereof, and supplies the voltage as the test voltage to the DUT from an output end of the first operational amplifier through the current/voltage converting means, and

the voltages are supplied as the common mode voltage and the detection voltage to the first current measuring means from the both ends of the current/voltage converting means.

3. The semiconductor testing apparatus according to claim 2, wherein the applied voltage source further supplies the reference voltage generated by the first DA converter to second current measuring means.

4. The semiconductor testing apparatus according to claim 1, wherein the applied voltage source comprises a first DA converter and reversal amplification buffering means,

the first DA converter generates a predetermined reference voltage based on set data which is set from the outside,

the reversal amplification buffering means is a reversal type operational amplifier for a power, receives the reference voltage, performs reversal amplification

upon receiving a test voltage which is supplied to the DUT, and supplies the voltage as the test voltage to the DUT from an output end of the reversal amplification buffering means through the current/voltage converting means, and

the voltages are supplied as the common mode voltage and the detection voltage from both ends of the current/voltage converting means to third current measuring means, and the reference voltage generated by the first DA converter is supplied to the third current measuring means.

5. The semiconductor testing apparatus according to claims 1 to 4, wherein each of the first to third current measuring means comprise offset voltage giving means, an AD converter and data storing means,

the offset voltage giving means switches and receives the common mode voltage and the detection voltage in time series, and outputs a first low-voltage signal corresponding to the common mode voltage and a second low-voltage signal corresponding to the detection voltage which are subjected to voltage shift to fall within a predetermined low-voltage range,

the AD converter receives the first low-voltage signal and the second low-voltage signal subjected to voltage shift to become low voltages in time series, and outputs first measurement data and second measurement data obtained by performing quantization conversion to each of the signals, and

the data storing means is a memory or a register

capable of storing at least one set of the first measurement data and the second measurement data.

6. The semiconductor testing apparatus according to claim 2, wherein the first current measuring means comprises first input signal switching means which receives the common mode voltage and the detection voltage of one system which are input to the current measuring means, switches to one of the voltages and outputs the switched voltage to the offset voltage giving means.

7. The semiconductor testing apparatus according to claim 3, wherein the second current measuring means comprises second input signal switching means which receives a plurality of groups of input signals each indicating a set of the common mode voltage and the detection voltage from a plurality of channels, switches to one of the plurality of groups and supplies the switched group to the offset voltage giving means.

8. The semiconductor testing apparatus according to claim 4, wherein the third current measuring means comprises third input signal switching means which receives a plurality of groups of input signals each indicating a set of the common mode voltage and the detection voltage from a plurality of channels, switches to one of the plurality of groups and supplies the switched group to the offset voltage giving means, and which also receives the set voltages from the first DA

converters of the plurality of channels, switches to the set voltage of a channel corresponding to the selected common mode voltage or detection voltage and supplies the switched set voltage to the offset voltage giving means.

9. The semiconductor testing apparatus according to claims 5 to 8, further comprising:

means for applying gradual voltages to both ends of each of at least the first resistance and the second resistance included in the offset voltage giving means in order to perform measurement before a test of the DUT;

means for specifying a deviation between the obtained non-linear characteristic data of the resistances and an ideal resistance; and

means for linearly correcting the common mode voltage and the detection voltage obtained by measuring a current flowing through the DUT based on the specified non-linear characteristics of the resistance so that the non-linear characteristics of the resistance become the ideal resistance.